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EXAMINER
THANGAVELU, KANDASAMY

ART UNIT	PAPER NUMBER
2123	14

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/273,560	Applicant(s) HASEGAWA, TAKUMI	
	Examiner Kandasamy Thangavelu	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Introduction

1. This communication is in response to the Applicant's request for reconsideration mailed on April 29, 2003. Claims 1-4 of the application are pending.

Response to Arguments

2. Applicants' arguments filed on April 29, 2003 have been fully considered. Applicants' arguments, filed on April 29, 2003 under 35 U.S.C. 103 (a) are not persuasive. Therefore, this office action is made final.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Blinne et al. (BL)** (U.S. Patent 5,274,568) in view of **Hasegawa (HAS)** (U.S. Patent 6,041,168) and further in view of **Hasegawa (HS)** (U.S. Patent 5,528,511).

5.1 **BL** teaches method of estimating logic cell delay time. Specifically, as per Claim 1, **BL** teaches the delay analysis system for delay analysis of a logic circuit (Col 1, Lines 7-13);

the system having a delay analysis library (Col 1, Lines 9-13);

containing connection information on a plurality of circuits (Col 1, Lines 39-40; Col 1, Lines 60-62);

and the delay time information on rises and falls of each input terminal and output terminal of the plurality of circuits (Col 1, Lines 45-48).

BL does not expressly teach the library further contains logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of the plurality of circuits. **HAS** teaches that the library further contains logical operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35), as delay verification time can be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information (Col 2, Lines 28-35). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** with the system of **HAS** that included the

library containing logical operation information, as delay verification time could be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information.

BL and **HAS** do not expressly teach the logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of the plurality of circuits. **HS** teaches that the logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of the plurality of circuits (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** and **HAS** with the system of **HS** that included the logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of the plurality of circuits, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

BL does not expressly teach that when making a delay analysis of the logic circuit including at least one of plurality of circuits, a delay time is selected from the delay time information according to a logical operation of one of the circuits. **HS** teaches that when making a delay analysis of the logic circuit including at least one of the plurality of circuits, a delay time is selected from the delay time information according to a logical operation of one of the circuits (Col 2, Lines 30-42; Col 3, Lines 5-26), as this provides correct delay time even when either of

rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** with the system of **HS** that included when making a delay analysis of the logic circuit including at least one of plurality of circuits, a delay time being selected from the delay time information according to a logical operation of one of the circuits, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

5.2 As per Claim 2, **BL** teaches the delay analysis system for delay analysis of a logic circuit (Col 1, Lines 7-13);

the system having a delay analysis library (Col 1, Lines 9-13);

containing connection information on a plurality of circuits (Col 1, Lines 39-40; Col 1, Lines 60-62);

and the delay time information on rises and falls of each input terminal and output terminal of the plurality of circuits (Col 1, Lines 45-48).

BL does not expressly teach the library further contains logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of the plurality of circuits. **HAS** teaches that the library further contains logical operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35), as delay verification time can be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information (Col 2, Lines 28-35). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** with the system of **HAS** that included the

library containing logical operation information, as delay verification time could be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information.

BL and **HAS** do not expressly teach the logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of the plurality of circuits. **HS** teaches that the logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of the plurality of circuits (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** and **HAS** with the system of **HS** that included the logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of the plurality of circuits, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

BL does not expressly teach that when making a delay analysis of the logic circuit, a delay time between the input terminal and the output terminal is selected from the delay time information according to a logical operation of one of the circuits. **HS** teaches that when making a delay analysis of the logic circuit, a delay time between the input terminal and the output terminal is selected from the delay time information according to a logical operation of one of the circuits (Col 2, Lines 30-42; Col 3, Lines 5-26), as this provides correct delay time even

when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** with the system of **HS** that included when making a delay analysis of the logic circuit, a delay time between the input terminal and the output terminal being selected from the delay time information according to a logical operation of one of the circuits, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

5.3 As per Claim 3, **BL** teaches a method for making a delay analysis of a logic circuit (Col 1, Lines 7-13); comprising the steps of:

referencing a delay analysis library (Col 1, Lines 9-13);

containing connection information on a plurality of circuits (Col 1, Lines 39-40; Col 1, Lines 60-62);

and the delay time information on rises and falls of each input terminal and output terminal of at least one of the plurality of circuits (Col 1, Lines 45-48).

BL does not expressly teach the library further contains logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of the plurality of circuits. **HAS** teaches that the library further contains logical operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35), as delay verification time can be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information (Col 2, Lines 28-35). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **BL** with the method of **HAS** that included the

library containing logical operation information, as delay verification time could be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information.

BL and **HAS** do not expressly teach the logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of the plurality of circuits. **HS** teaches that the logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of the plurality of circuits (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **BL** and **HAS** with the method of **HS** that included the logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of the plurality of circuits, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

BL does not expressly teach selecting the delay time of at least one of the circuits from the delay time information according to a specified logic operation of the circuit. **HS** teaches selecting the delay time of at least one of the circuits from the delay time information according to a specified logic operation of the circuit (Col 2, Lines 30-42; Col 3, Lines 5-26), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary

skill in the art at the time of Applicant's invention to modify the method of **BL** with the method of **HS** that included selecting the delay time of at least one of the circuits from the delay time information according to a specified logic operation of the circuit, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

5.4 As per Claim 4, **BL** teaches a computer-readable medium having stored thereon a program for executing a process step (Col 2, Lines 42-50); comprising:

referencing a delay analysis library (Col 1, Lines 9-13);

containing connection information on a plurality of circuits (Col 1, Lines 39-40; Col 1, Lines 60-62);

and the delay time information on rises and falls of each input terminal and output terminal of each one of the plurality of circuits (Col 1, Lines 45-48).

BL does not expressly teach the library further contains logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of each one of the plurality of circuits. **HAS** teaches that the library further contains logical operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35), as delay verification time can be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information (Col 2, Lines 28-35). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer-readable medium of **BL** with the computer-readable medium of **HAS** that included the library containing logical operation information, as delay verification time could be shortened and high speed delay verification

achieved by calculating delay time based on logic information, connecting information and delay information.

BL and **HAS** do not expressly teach the logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of the plurality of circuits. **HS** teaches that the logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of the plurality of circuits (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer-readable medium of **BL** and **HAS** with the computer-readable medium of **HS** that included the logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of the plurality of circuits, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

BL does not expressly teach selecting the delay time of at least one of the circuits from the delay time information according to a logic operation of the circuit. **HS** teaches selecting the delay time of at least one of the circuits from the delay time information according to a logic operation of the circuit (Col 2, Lines 30-42; Col 3, Lines 5-26), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer-readable medium of **BL** with the

computer-readable medium of **HS** that included selecting the delay time of at least one of the circuits from the delay time information according to a logic operation of the circuit, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

BL does not expressly teach a computer-readable medium having stored thereon a program for executing a process step of performing a delay calculation using selected delay time as a propagation delay time of at least one of circuits. **HS** teaches a computer-readable medium having stored thereon a program for executing a process step of performing a delay calculation using selected delay time as a propagation delay time of at least one of circuits (Col 3, Lines 5-26), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer-readable medium having stored thereon a program of **BL** with the computer-readable medium having stored thereon a program of **HS** that included executing a process step of performing a delay calculation using selected delay time as a propagation delay time of at least one of circuits, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

Applicants' Arguments

6. The applicant argues the following:

(1) the combination of Blinne, Hasegawa'168 and Hasegawa'511 does not teach or suggest all of the claimed features of the applicant's invention;

(2) Hasegawa '168 does not disclose that the logical operation information is stored in a delay analysis library as required by the claim; Hasegawa '168 does not disclose a delay analysis library at all; nothing in either Blinne or Hasegawa would suggest that logical operation information be stored in the cell library of Blinne;

(3) Hasegawa '168 does not disclose logical operation information representing a correspondence between a logical value of each input terminal and the logical value of the output terminal as required by claim 1;

(4) In Hasegawa '168, the logical values of the terminals are not used in delay time calculation at all; and

(5) each of Blinne, Hasegawa '168 and Hasegawa'511 disclose a fully functional system for determining the delay time of a logic circuit that is incompatible with others and there would be no motivation to combine the references at all; it is likely that combining the parts of the system of one reference with those of another could render the delay analysis system inoperable.

Examiner's reply

7. As per the Applicants' arguments, the Applicants' attention is requested to the corresponding claim rejections. In addition, the following explanation is provided to further explain the examiner's position.

7.1 In response to the Applicants' argument that "the combination of Blinne, Hasegawa'168 and Hasegawa'511 does not teach or suggest all of the claimed features of the applicant's

invention", the examiner requests the applicant's attention to the references provided in the claim rejections for Claims 1-4.

7.2 In response to the Applicant's argument that "Hasegawa '168 does not disclose that the logical operation information is stored in a delay analysis library as required by the claim; Hasegawa '168 does not disclose a delay analysis library at all; nothing in either Blinne or Hasegawa would suggest that logical operation information be stored in the cell library of Blinne", the examiner respectfully disagrees. Hasegawa '168 refers to delay model storing means (Col 1, Lines 58-67). Hasegawa '168 teaches that the delay model storing means stores information of a circuit model including logic information, connecting information and delay information of the logic circuit (Col 1, Lines 62-61). The examiner contends that this delay model storing means is the delay analysis library. Blinne teaches estimating the delay times of the integrated circuit logic cells using cell libraries (Col 1, Lines 7-13; and Col 2, Line 62 to Col 3, Line 6). So it would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the model storing means of Hasegawa '168 with the cell library of Blinne, so delay time can be calculated for each pin based on the information on the circuit model such as logic information, connecting information and delay information (HAS: Col 2, Lines 30-35).

7.3 In response to the Applicant's argument that "Hasegawa '168 does not disclose logical operation information representing a correspondence between a logical value of each input terminal and the logical value of the output terminal as required by claim 1", the examiner

requests applicants attention to Hasegawa '511 (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42). The logical operation information can be represented in waveform or truth tables. Hasegawa '511 discusses the logical operation information with reference to an OR gate and shows how it is represented in the waveform.

7.4 In response to the Applicant's argument that "In Hasegawa '168, the logical values of the terminals are not used in delay time calculation at all", the examiner requests applicants attention to the fact that the examiner had used Hasegawa '511, which uses the logical operation information in calculating the delay times (Col 2, Lines 30-42; Col 3, Lines 5-26). Hasegawa uses the logical operation information to generate the arc invalidness and validness. Then he uses this information to calculate the delay times.

7.5 In response to the Applicant's argument that "each of Blinne, Hasegawa '168 and Hasegawa'511 disclose a fully functional system for determining the delay time of a logic circuit that is incompatible with others and there would be no motivation to combine the references at all; it is likely that combining the parts of the system of one reference with those of another could render the delay analysis system inoperable", the examiner respectfully disagrees. Blinne teaches a method of calculating the delay times of integrated circuit cells using cell library (Col 1, Lines 7-13; Col 2, Line 62 to Col 3, Line 6). Hasegawa '168 calculates for each pin the delay time based on the contents of the delay model storing means, which contains logic information, connecting information and delay information Col 2, Lines 30-35). Hasegawa '511 shows how the logic information could be stored (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42) and how it

can be used to compute the delay times (Col 2, Lines 30-42; Col 3, Lines 5-26). So the examiner maintains that the three references could be combined to achieve the claimed elements of the applicant's invention and it will be operable.

Conclusion

ACTION IS FINAL

8. Applicants' arguments with respect to claim rejections under 35 USC § 103 (a) are not persuasive. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is

703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7329.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
June 11, 2003

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER